REMARKS

Summary of Office Action

Claims 1-20 were pending in the above-identified patent application.

Claims 1-20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Rangasayee U.S. Patent No. 6,404,225 (hereinafter "Rangasayee").

Reconsideration of this application in light of the following remarks is hereby respectfully requested.

Summary of Applicant's Reply

Applicant has amended the specification to correct a minor typographical error. Applicant has also amended claims 1, 2, 9, and 14 to more particularly define the claimed invention. Applicant has canceled claims 3, 4, and 10 without prejudice. No new matter has been added and the amendments are fully supported by the originally filed specification (see, e.g., applicant's specification at FIG. 3; pp. 3-4, ¶¶ 8-9; pp. 7-8, ¶¶ 18-19; and p. 11, ¶ 28). The Examiner's rejections are respectfully traversed.

Applicant's Reply to the Rejection Under 35 U.S.C. § 102(b)

Claims 1, 2, 5-9, and 11-20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Rangasayee.[1] The Examiner's rejections are respectfully traversed.

---

[1] Claim 1 was amended to incorporate the features of cancelled claims 3 and 4. Claim 9 was amended to

(Continued...)

Applicant's claimed invention is directed to improving connectivity between signaling input/output (I/O) and an intellectual property (IP) block in a programmable logic resource. A programmable logic resource having a plurality of I/O ports located along its periphery is embedded in a package having a plurality of pins, which is mounted on a printed circuit board at fixed pin locations. As described in the Background of the Invention section of the specification, data from external circuitry is typically sent to the programmable logic resource through a particular pin to a corresponding I/O port where the data is decoded and then sent to a corresponding data port in the IP block for processing. (Applicant's specification at pp. 1-2, ¶¶ 3-4).

Connectivity problems arise when a board vendor designs a circuit board having fixed pin connections that support a particular package in which a programmable logic resource is embedded. Because the programmable logic resource can come in different sizes, the locations of the I/O ports and corresponding data ports at the IP block of the programmable logic resource change relative to the pin locations for the particular package. To accommodate a particular programmable logic resource, extra wiring is typically used to route data between a

---

(...Continued)
incorporate the features of cancelled claim 10. In addressing the rejection of claims 1 and 9, applicant will address the Examiner's rejections with respect to claims 1, 3, 4, 9, and 10.

pin to a corresponding I/O port. However, this can be limited by the available space for the extra wiring, can cause additional delay times, and can cause further connectivity problems. (Applicant's specification at pp. 2-3, ¶ 5).

In accordance with the invention, at least one of the pins on the package sends data to a nearest available I/O port on the programmable logic resource such that the pin corresponds to other than the nearest available I/O port. This data is decoded in an I/O buffer and sent as input to a crossbar switch that can be configured to send the data to a corresponding data port in the IP block for processing (Applicant's specification at pp. 3-4, ¶¶ 7-9; pp. 7-8, ¶¶ 20-21; and independent claims 1, 9, and 14).

Rangasayee describes an integrated circuit capable of operating in a plurality of switching modes. A programmable logic device operates as a programmable switching device having a plurality of interconnection lines, bi-directional I/O ports connected to external circuitry, and a programmable function block that can be programmably connected to the I/O ports. The programmable logic device also includes a programmable switch unit having two sets of I/O lines such that a selected portion of the first set of I/O lines can be directed by the programmable function block to connect with a selected portion of the second set of I/O lines. This improves the internal routing of signals within the programmable logic device to support the plurality of switching modes. (Rangasayee at Abstract; col. 2, l. 66

to col. 3, l. 50; and col. 4, l. 49 to col. 5, l. 48).

Although applicant's claimed invention may generally implicate the subject matter of Rangasayee, applicant's claimed invention patentably improves upon Rangasayee by providing a programmable logic resource having I/O ports located along its periphery and embedded in a package having a plurality of pins where at least one of the pins is coupled to a nearest available one of the I/O ports such that the pin corresponds to other than the nearest available I/O port as recited in applicant's independent claims 1, 9, and 14. Applicant's claimed invention patentably improves upon Rangasayee by improving the external routing of signals from the pins of the package to the I/O ports of the programmable logic resource.

For at the foregoing reasons, applicant respectfully submits that independent claims 1, 9, and 14, as amended, are allowable over Rangasayee. Claims 2, 5-8, 11-13, and 15-20, which depend from respective independent claims 1, 9, and 14, are therefore also allowable over Rangasayee.

Conclusion

Applicant respectfully submits that this application is now in condition for allowance. Accordingly, prompt consideration and allowance of this application are respectfully requested.

Respectfully Submitted,

Evelyn C. Mak

Evelyn C. Mak
Registration No. 50,492
Attorney for Applicant

FISH & NEAVE IP GROUP
ROPES & GRAY LLP
Customer No. 36981
1251 Avenue of the Americas
New York, New York 10020-1105
(212) 596-9000